Paper No. 21

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JACK H. LINN, ROBERT K. LOWRY and GEORGE V. ROUSE

Appeal No. 2002-1981
Application No. 09/316,580

ON BRIEF

Before BAHR, BLANKENSHIP, and POTEATE, Administrative Patent Judges.

POTEATE, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal under 35 U.S.C. § 134 from the final rejection of claims 1-5, 7-10 and 13-22. Claims 1 and 7 are representative of the subject matter on appeal and are reproduced below:

1. A silicon-on-insulator integrated circuit, comprising:

(a) a handle die;

(b) a substantially continuous silicide layer over said handle die;

(c) a substantially continuous first dielectric layer overlying one side of said silicide layer;

(d) a device silicon layer overlying said first dielectric layer, said device silicon layer having an upper surface;

(e) a second dielectric layer on said handle die underlying the opposite side of said silicide layer; and

(f) interconnected transistors in and at the upper surface of said device silicon layer.

7. A silicon-on insulator integrated circuit comprising:

(a) a handle die;

(b) a first dielectric layer formed on said handle die

(c) a substantially continuous silicide layer formed on said first dielectric layer, said silicide layer having a controlled resistance and providing a diffusion barrier to impurities;

(d) a substantially continuous second dielectric layer disposed between said silicide layer and a device silicon layer;

(e) trenches extending through said device silicon layer and silicide layer and separating said device silicon layer into islands each with an underlying continuous silicide area; and

(f) interconnected transistors in and at an upper surface of said device silicon layer.

The references relied upon by the examiner are:

Moslehi	5,102,821	Apr. 7, 1992
See et al. (See)	5,212,397	May 18, 1993
Ochiai	5,378,919	Jan. 3, 1995
Kameyama et al. (Kameyama)	64-73659	Mar. 17, 1989

Sugimoto et al. (Sugimoto) 2-206118 Aug. 15, 1990

We note that the examiner has relied upon abstracts of foreign references in his prior art rejections of the claims. In the future, the examiner should ensure that any prior art rejections are based on the complete translation of the entire foreign document.

Grounds of Rejection[1]

1. Claims 4, 5, 10 and 13-22 stand rejected under 35 U.S.C. § 112, first paragraph.

We affirm.

2. Claims 10 and 13 stand rejected under 35 U.S.C. § 112, second paragraph.

We affirm.

3. Claims 1-4 stand rejected under 35 U.S.C. § 103 as unpatentable over Moslehi in view of See.

We reverse.

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[1]The examiner has withdrawn several grounds of rejection which may be found on pages 2-3 of the examiner's answer, Paper No. 17, mailed December 12, 2001. In addition, the examiner has entered appellants' amendment canceling claim 11, which amendment was filed on May 24, 2001. Id., page 2.

4. Claim 5 stands rejected under 35 U.S.C. § 103 as unpatentable over Moslehi in view of See and further in view of Sugimoto.

We reverse.

5. Claims 7-9 stand rejected under 35 U.S.C. § 103 as unpatentable over Ochiai in view of Kameyama.

We reverse.

We also note that the examiner has raised an objection to the specification under 35 U.S.C. § 132. See examiner's answer, page 8-page 9. The appellants do not indicate that the Section 132 objection is an issue on appeal (see revised appeal brief, Paper No. 13, received May 24, 2001, page 5, hereinafter "appeal brief"), however, appellants do present arguments in response to this objection. Appeal to the Board of Appeals may only be taken from a decision of the examiner twice or finally rejecting claims. See 37 CFR § 1.191. We consider the objection raised by the examiner only to the extent that it relates to issues raised in connection with the claims on appeal. We have concluded that the alleged new matter does not appear to relate to these issues.

Background

The invention relates to dielectrically isolated semiconductor integrated circuits and methods of fabrication. Specification, page 1, lines 14-16. According to appellants, the invention provides silicon-on-insulator bonded wafer processing which has numerous advantages over conventional processes. See Specification, page 4, lines 12-20.

Discussion

For purposes of this appeal, appellants indicate that the following groups of claims stand or fall together: (1) claims 1-3, (2) claims 4-5, (3) claims 7-9, (4) claims 10, 13-15 and 22, (5) claims 16-18 and (6) claims 19-21. Appeal brief, page 6.

1. Rejection of claims 4, 5, 10 and 13-22 under 35 U.S.C. § 112, first paragraph

Claims 4 and 5

Appellants argue that the subject matter of claims 4 and 5 is supported on page 7, lines 22-29 of the specification and in Figure 4a. See examiner's answer, page 13. It is the examiner's position that claim 1, from which these claims depend, only reads on the structure disclosed in Figure 3 while the subject matter of claims 4 and 5 relates to the structure disclosed in Figure 4.

Id. Appellants do not appear to dispute the examiner's contention and, in fact, indicate that they have previously proposed changing the dependencies of claims 4 and 5 to claim 7, which reads on the structure shown in Figure 4. See appeal brief, page 6.

As appellants do not present arguments traversing the examiner's position, the rejection is affirmed.

Claim 10

It is the examiner's contention that the specification does not support the presence of first, second and third bonding materials in the final bonded wafer structure of claim 10. See examiner's answer, pages 14-15. In support of their contention that the specification does teach three bonding materials, appellants reference Figures 5A and B and the disclosure in the specification relating to the formation of nitrox 519 by reaction of oxidizer drop 505 with polysilicon 514. Appeal brief, pages 8-9.

We have reviewed the referenced portion of the specification and note that while first and second bonding materials are initially utilized, they are ultimately consumed by the reaction to form nitrox, such that only a single bonding zone remains in the final structure. See specification, pages 9-10.

Accordingly, we are in agreement with the examiner that the specification does not support the presence of three bonding materials in the final, claimed bonded wafer integrated circuit.

The rejection is affirmed.

Claim 13

According to the examiner, the specification fails to disclose that the first dielectric layer is silicon dioxide as recited in claim 13. Examiner's answer, page 15. We agree. The portion of the specification referenced by appellants as supporting this claim limitation (specification, page 9, lines 7-13) states only that the handle wafer 512 is oxidized to form *oxide* layer 513. The specification fails to teach that this layer is silicon *dioxide*.

The rejection is affirmed.

Claims 15 and 17

Claims 15 and 17 depend from claim 10. According to the examiner, none of the embodiments disclosed in the specification discloses structure having the elements of claims 10 and 15 or of claims 10 and 17. See examiner's answer, page 15. Appellants argue that page 11, lines 2-16 and Figure 6 support the limitations in these claims. Appeal brief, page 9. Based on our review of the referenced portions of the specification, we are in

agreement with the examiner's findings that the specification does not support the claimed structures.

The rejection is affirmed.

Claim 19

Claim 19 requires that the first and second bonding materials each comprise a thin layer of polysilicon, the polysilicon being substantially consumed during bonding. We are in agreement with the examiner's position that this claim language is not supported by the specification for the same reasons discussed above in connection with claim 10.

The rejection is affirmed.

Claim 22

In support of their position that claim 22 is supported by the specification, appellants reference page 10, lines 28-32, of the specification which indicates that the metal of any of the three disclosed embodiments may be replaced with a silicide. However, we are in agreement with the examiner that the specification only supports the third bonding material as being directed to the oxidizer 505.

The rejection is affirmed.

The rejection under 35 U.S.C. § 112, first paragraph, as to the remaining claims 14, 16, 18, 20 and 21 is also affirmed as

appellants have failed to present separate arguments in response to the examiner's rejection of these claims.

2. Rejection of claims 10 and 13 under 35 U.S.C. § 112, second paragraph

Appellants do not appear to traverse this ground of rejection. Rather, appellants note that they have previously proposed amending claim 10 to reword line 11 to more clearly describe the bonding of the silicide layer to the handle die and device wafer. Appeal brief, page 6. Appellants also note that their proposed amendment to claim 13 (paper no. 6, received March 13, 2000) to insert an open bracket which was previously inadvertently admitted was not entered. Id.

As appellants have failed to traverse the merits of the examiner's rejection, the rejection is affirmed.

3. Rejection of claims 1-4 under 35 U.S.C. § 103 as unpatentable over Moslehi in view of See

The examiner found that Moslehi discloses the structure as claimed with the exception that Moslehi does not show transistors formed on the Si substrate. Examiner's answer, page 10. The examiner relies on See solely for a teaching of bipolar and MOS transistors formed on an Si substrate. Id.

Appellants' principle argument is that Moslehi fails to teach "the substantially continuous first dielectric layer overlying one side of said silicide layer" as required by claim 1. Appeal brief, page 10. In this regard, appellants point out that in the Moslehi structure, the layer overlying the oxide layer 22 contains both a silicide 40 and a metal 24 in a grid pattern. Id.

The examiner, on the other hand, takes the position that while claim 1 recites a "substantially continuous silicide layer over the handle die," the claim never requires a "continuous unpatterned silicide layer over the handle die." Examiner's answer, page 16. The examiner maintains that "[s]ince the polycrystalline silicon layer [38] is a continuous, grid-patterned layer, the $TiSi_2$ (titanium silicide) layer [40] is also a continuous, grid-patterned layer formed on the handle die [20]." Id.

In determining what is meant by words in a claim, we look to the specification. See In re Cruciferous Sprout Litigation v. Sunrise Farms, 301 F.2d 1343, 1348, 64 USPQ2d 1202, 1205 (Fed. Cir. 2002). We have reviewed the specification and are in agreement with appellants that the claim language "a

substantially continuous first dielectric layer" clearly defines over Moslehi's grid structure.

As the combined teachings of Moslehi and See fail to disclose or suggest this claim feature, we find that the examiner has failed to established a prima facie case of obviousness and the rejection is reversed.

4. Rejection of claim 5 under 35 U.S.C. § 103 as unpatentable over Moslehi in view of See and Sugimoto

The examiner relies on Sugimoto for the disclosure of a dielectric layer made of diamond. However, we have concluded that Sugimoto fails to remedy the deficiency in the combined teachings of Moslehi and See discussed in connection with claim 1, from which claim 5 depends. In particular, Sugimoto fails to disclose or suggest a substantially continuous first dielectric layer overlying one side of the silicide layer as required by claim 1.

Accordingly, the rejection is reversed.

5. Rejection of claims 7-9 under 35 U.S.C. § 103 as unpatentable over Ochiai in view of Kameyama.

The examiner found that Ochiai discloses the invention as claimed with the exception of a teaching that the resistance layer is made of silicide. The examiner relies on Kameyama as

disclosing a tungsten silicide resistor and maintains that it would have been obvious to have used the resistor of Kameyama in Ochiai's device because it is a widely used resistance material. Examiner's answer, page 11.

Appellants argue that Ochiai teaches a "sea-of-gate array" and, therefore, includes no trenches to define islands as required by claim 7, paragraph (e). See appeal brief, page 12. Appellants also note that Kameyama discloses a patterned polycrystalline tungsten silicide resistor thin film which does not meet the limitation that the silicide layer is "substantially continuous." Id.

We find that the Examiner's attempt to equate Ochiai's structure with the claimed trenches which extend through the device silicon layer and silicide layer and separate the device silicon layer into islands is clearly based on improper hindsight reasoning. See W.L. Gore & Assocs. v. Garlock, 721 F.2d at 1553, 222 USPQ at 312-13. The rejection is reversed.

Time Period For Response

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

JENNIFER D. BAHR
Administrative Patent Judge

HOWARD B. BLANKENSHIP
Administrative Patent Judge

LINDA R. POTEATE
Administrative Patent Judge

BOARD OF PATENT APPEALS AND INTERFERENCES

LRP/lbg

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